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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/987,012	11/13/2001	Kenichi Watanabe	011264	6363

23850 7590 03/15/2004

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EXAMINER

CHU, CHRIS C

ART UNIT	PAPER NUMBER
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2815

DATE MAILED: 03/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/987,012

Applicant(s)

WATANABE, KENICHI

Examiner

Chris C. Chu

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 17 December 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1 - 22 is/are pending in the application.
- 4a) Of the above claim(s) 2 - 20 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1, 21 and 22 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 12/17/04 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Request for Continued Examination

1. A request for continued examination (RCE) under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on December 17, 2003 has been entered. An action on the RCE follows.

Response to Amendment

2. Applicant's amendment filed on November 12, 2003 has been received and entered in the case.

Election/Restrictions

3. Claims 2 - 20 continue to be withdrawn from consideration for the reasons provided in the Office action mailed on August 1, 2003.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(e) the invention was described in-

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(1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or

(2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

5. Claims 1, 21 and 22 are rejected under 35 U.S.C. 102(e) as being anticipated by Iguchi '363.

Regarding claim 1, Iguchi discloses in Fig. 1, Fig. 3, Fig. 5(a), Fig. 5(b), Fig. 15, Fig. 17, column 8, lines 38 - 67 and column 12, lines 14 - 22 a semiconductor wafer device comprising:

- a semiconductor wafer (a structure in Fig. 17) comprising a circuit area (25 and 51) disposed in a central area of said semiconductor wafer and a peripheral area (26 and 50) of said semiconductor wafer not formed with circuits;
- a number of semiconductor elements (elements in the area 25 which is sectioned into with scribe lines) formed in said circuit area;
- a circuit multi-layer wiring structure (5 and 6) formed in said circuit area and comprising multi-layer wirings connected to said semiconductor elements and interlevel insulating films (2, 3 and 7), at least some of said multi-layer wirings being damascene wirings including wiring patterns and via conductors embedded in said interlevel insulating films; and
- a peripheral multi-layer structure (21) formed in said peripheral area, comprising insulating films (2, 3 and 7) made of a same materials as said interlevel insulating films and one or more conductor filled trenches forming conductor patterns (the dark and "J" shaped structure in 21), defined between sidewalls of said insulating films

(2, 3 and 7), made of same materials as said wiring patterns and not having conductor patterns corresponding to said via conductors.

Regarding claim 21, Iguchi discloses in Fig. 1, Fig. 5(a), Fig. 5(b), Fig. 15 and column 12, lines 14 - 22 a semiconductor wafer device, comprising:

- an underlying structure (1) including a semiconductor wafer;
- a first insulating layer (2) having a lower dielectric constant than silicon oxide and formed over said underlying structure in an area excepting a peripheral area of said underlying structure;
- a second insulating layer (3) having a dielectric constant higher than said first insulating layer and formed on said first insulating layer;
- wiring grooves (at the place of 5) formed at least through said second insulating layer;
- patterns of conductor filled (6) in said wiring grooves;
- said second insulating layer or a layer (the dark and “J” shaped structure in 21) of a same material as the conductor covering an outermost side wall of said first insulating layer, and wherein
- a multi-layer peripheral structure (21) is formed in said peripheral area not formed with circuits, comprising one or more conductor filled trenches forming conductor patterns (the dark and “J” shaped structure in 21).

Regarding claim 22, Iguchi discloses in Fig. 1, Fig. 3, Fig. 5(a), Fig. 5(b), Fig. 15, Fig. 17, column 8, lines 38 - 67 and column 12, lines 14 - 22 said interlevel insulating films (2, 3 and 7) including a first insulating layer (2) having a lower dielectric constant than silicon oxide and formed over said semiconductor wafer in an area except said peripheral area, and a second

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insulating layer (3) having a dielectric constant higher than said first insulating layer and formed on said first insulating layer and said device further comprising said second insulating layer or a layer (7) of a same material as the conductor covering an outermost side wall of said first insulating layer.

Response to Arguments

6. Applicant's arguments filed November 12, 2003 have been fully considered but they are not persuasive.

On page 15, applicant argues "The language 'conductor filled trenches' means that the conductor is filled in the trench, which trench is a recessed portion or groove, previously made. This is clearly different from Iguchi, which discloses a metal residue formed at a stepped portion of one insulating layer, where the next insulating layer covers the metal residue. Iguchi does not disclose forming conductor filled trenches, as required by the presently amended claims". This argument is not persuasive. Since applicant does not specifically claimed that the trench is formed in one insulating layer, it is irrelevant that the trench is formed by one layer or multi-layers. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Thus, Iguchi clearly shows in e.g., Fig. 1 conductor (the dark and "J" shaped structure in 21) filled trenches (at the place of the dark and "J" shaped structure in 21).

For the above reasons, the rejection is maintained.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chris C. Chu whose telephone number is 571-272-1724. The examiner can normally be reached on 11:30 - 8:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 517-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

c.c.
3/4/04 12:49:12 PM

A handwritten signature in black ink, appearing to read 'Bradley Baumeister', with a stylized, cursive script.

**BRADLEY BAUMEISTER
PRIMARY EXAMINER**